

ARTICLE

PNR: A Complete 28nm Physical Design Case Study Using Synopsys ICC2

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Abstract

The 28nm technology node remains an important component in present-day VLSI design because it provides a useful trade-off between power efficiency and fabrication cost. However, at this geometry, transforming a gate-level netlist into a signoff-compliant GDSII layout presents major physical design challenges that must be handled through optimization. A case study of the Physical Implementation (Place and Route) flow using the Synopsys IC Compiler II (ICC2) tool and a 28nm planar MOSFET technology is described. The paper explores methods to address high design density with a focus on power, performance, and area. With reduced feature size, routing congestion and interconnect delays become critical factors. Placement techniques such as congestion-aware placement, Concurrent Clock and Data optimization, and Multi-Corner Multi-Mode analysis are used to achieve timing closure. The work also investigates signal integrity, IR drop, layout-dependent effects, and provides a quantitative PPA analysis for reliable silicon signoff at 28nm.

Keywords: 28nm Planar CMOS, Interconnect-Dominated Design, Physical Design, Place and Route, Routing Congestion, RTL-to-Signoff Flow, VLSI Physical Implementation

Abbreviations: ASIC: Application-Specific Integrated Circuit, CCD: Concurrent Clock and Data, CMOS: Complementary Metal Oxide Semiconductor, CTS: Clock Tree Synthesis, DRC: Design Rule Check, DRV: Design Rule Violation, EM: Electromigration, HFNS: High-Fanout Net Synthesis, LVS: Layout Versus Schematic, MCM: Multi-Corner Multi-Mode, PnR: Place and Route, SI: Signal Integrity, SoC: System-on-Chip, VLSI: Very-Large-Scale Integration

1. Introduction

The further scaling of semiconductor technology has made possible the construction of extremely complex System-on-Chip (SoCs), which have increased performance and functionality with strong power, area, and cost requirements. 16nm FinFET technologies are the most important technologies in high-performance computer technologies, whereas 28nm planar CMOS is a fundamental and extensively used technology in the semiconductor industry. It's highly matured nature, predictable manufacturing properties, good balance of performance, power efficacy and fabrication cost are the reasons why the choice of high volume products including electronics, networking infrastructure and automotive systems. This means that the physical implementation at the 28nm node is still practically relevant and technically difficult to accomplish with reliable and sign-off-clean physical implementation in current VLSI design.

1.1 Why End-to-End Physical Design Is Critical at the 28nm Node

The most important part of the ASIC design flow is Physical Design which is the process in which gate-level netlist is translated into physical layout to meet the specifications of timing, power, signal integrity, and reliability. Further aggressive reduction of geometries and design density at the 28nm technology node exacerbates the effects of interconnect parasitics, routing congestion and power integrity constraints. Delays caused by interconnect, resistance-capacitance (RC) and coupling noise effects are no longer secondary performance considerations, but rather decisive in determining circuit behaviour as in the earlier nodes, the gate delay was. As a result, normal optimization techniques are not sufficient for achieving timing closure, it is necessary to consider the whole, end-to-end methodology in which placement, clock tree synthesis, routing, and timing analysis are integrated to manage the trade-offs between Power, Performance, and Area.

1.2 Bridging Academic Models and Industrial Physical Design Workflows

Algorithms applied to a full industrial sign-off flow have little connection with the literature on academic studies of individual algorithms used to place or route separately. In a practical industrial design, designers need to deal with simultaneous problems that are not simplified in the theoretical models, including Layout Dependent Effects (LDE), signal integrity degradation due to crosstalk, and Multi-Corner Multi-Mode (MCM) conditions. In addition, the interaction between the Power Delivery Network (PDN) and routing resources is often neglected in theoretical investigations, although the PDN takes a large share of the available metal layers and has a direct effect on congestion. The way to fill this gap is to use a methodology that would take advantage of state-of-the-art Electronic Design Automation (EDA) tools such as Synopsys IC Compiler II (ICC2) to consider these nanometer-scale effects in a single, sign-off-aware environment. Earlier algorithmic and analytical studies on placement, routing, and constraint handling form the theoretical basis of modern industrial physical design flows, even though many simplifying assumptions made in academic models do not hold in signoff-driven environments [1].

1.3 Justification for a Complete 28nm RTL to Signoff Flow Analysis

The reason behind this work can be attributed to the necessity of offering a clear, reproducible, and industry-standard roadmap on the implementation of 28nm. With an increase in the complexity of design, engineers need more than theoretical information, they need practical experience on how sophisticated methods like Concurrent Clock and Data (CCD) optimization, and congestion-conscious placement will behave during the floorplanning to physical verification. Through the capture of a full Place and Route (PnR) flow, this work aims to show how the limitations imposed by interconnect can be alleviated, and power integrity, such as reduction of IR drops and electromigration compliance, can be achieved, which are the key to first-pass silicon success. This paper presents a detailed case study of a 28nm planar CMOS design created in Synopsys ICC2 and gives a step-by-step account of the entire physical implementation process, starting with floorplanning and power grid design, and ending with final physical verification. The article emphasizes the use of higher order optimization techniques such as CCD optimization and MCM analysis to have strong timing closure when operating in real conditions. Moreover, the paper also offers an enhanced quantitative assessment of Power, Performance, and Area parameters, which offers practical proof of the efficiency of the selected methodologies. This work provides a useful guide to engineers and researchers who must cope with the challenges of reliable silicon sign-off at the 28nm node by overcoming the gap between theory and design reality.

2. Design Overview

In this section, the design features, technology setting, limitations, and the implementation approach that have been used in the case of physical design are outlined in this work. The aim is to design a transparent and repeatable experimental design that represents real-life industrial situation with a 28nm physical implementation flow, without revealing trade secrets of the design.

2.1 Structural Overview of the PNR Implementation Block

The design to be studied is called pnrblock, which is a synchronous digital block designed to be used in timing optimization through repeat insertion in a larger system-on-chip (SoC) context. pnrblock is functionally similar to work on timing closure, buffering long interconnect paths, and restructuring them to achieve timing closure, and is typical of the challenges of interconnect-dominated designs that are often found in nanometer-scale designs. The block has a single main synchronous clock and has internally generated clocks, creating further complexity in clock definition, propagation and timing analysis. The generated clocks must be closely synchronized with the launch and capture clocks, especially when the analysis is performed on multi corner timing and the necessity of a signoff based physical design methodology. Physically, pnrblock has six hard macros which have hard location requirements and have a major impact on floorplanning, routing congestion, and power grid planning. Together with the repeater-intensive property of the block, these properties render pnrblock an appropriate candidate in testing the congestion-aware placement, buffering schemes, and timing optimization that is conscious of physical factors. The design is complex enough to represent physical design constraints of the real world industrial, although implemented as a sub-block of a more complex SoC, as opposed to simplistic academic standards.

2.2 Process Technology and Design Complexity

It is implemented with a 28nm planar CMOS technology, which is chosen because it is still relevant in high-volume and low-cost applications. The design employs standard-cell libraries which use 28nm in the industry with multiple threshold voltage. Since pnrblock is a power constrained block, the primary use of this block is Standard Threshold Voltage (SVT) and High Threshold Voltage (HVT) cells to trade timing constraints with leakage power. The design has around 66.4k standard cells in the netlist. After placement, clock tree synthesis, and routing, the final design contains almost 75k standard cells after the addition of inverters, buffers required for timing, signal integrity, and signoff closure. Such growth in the number of cells is typical of deep-submicron physical implementation, in which interconnect-driven optimizations can have a substantial effect on end-design complexity [2]. The result of physical design is sensitive to interconnect parasitances, routing resource consumption, and power integrity effects, which is why the selected technology node is suitable in the context of investigating end-to-end PnR methodologies.

2.3 Performance and Power Constraints

The target pnrblock clock period is 2.2 ns, which translates into an operating frequency of around 454.5 MHz. This performance target, combined with the use of generated clocks, requires close management of clock skew, latency and uncertainty in the flow of the implementation. This block is set to work with a nominal supply voltage of 0.99 V and it is analysed in a Multi-Corner Multi-Mode (MCMM) framework. Representative RC and clock boundary conditions are said to represent the differences in interconnect behaviour and timing sensitivity in different operating conditions. Figure 4 represents the operating corners defined in the standard-cell library, including variations in process, voltage, and temperature. These operating conditions form the basis for Multi-Corner Multi-Mode (MCMM) analysis and ensure that timing, power, and reliability are evaluated under realistic worst-case and best-case scenarios. This analysis in MCMM makes timing closure robust

instead of optimized at one corner, as is consistent with signoff practices in industries [3]. The pnrblock is considered a power constrained block in terms of power. There are no multiple voltage domains or power gating systems used and the power intent is simpler with a greater focus on threshold voltage choice, buffering techniques and clock optimization. The use of SVT and HVT cells is mostly a choice of trade-off between the level of performance and leakage control, particularly in designs with many repeaters.

2.4 Signoff-Driven Physical Implementation Flow

The actual pnrblock implementation is based on a full Place and Route (PNR), signoff-focused physical implementation flow with an industry standard physical design implementation tool. The process starts with floorplanning, in which macro placement and core usage is determined to reconcile routability and timing feasibility requirements and power distribution requirements. Placement optimization is performed with congestion awareness, after that clock tree synthesis that accounts for both the main clock and the clocks that are generated from the main clock. The optimization of concurrent Clock and Data (CCD), is used to enhance the convergence of timing by enabling clock and data paths to be optimized simultaneously, which is highly applicable in interconnect-dominated designs [2]. The timing-driven and signal-integrity-conscious approaches are used to minimize crosstalk and unreasonable RC delay to implement routing. Post-route optimization aims at solving residual setup and hold violations in every MCM case, without compromising power integrity or electromigration reliability. Final physical verification is a test that establishes that the design satisfies timing, power, and reliability requirements that are required to be signed off. Figure 1 illustrates the signoff-driven end-to-end physical design flow adopted in this work, highlighting the interaction between timing, congestion, power integrity, and physical verification stages.

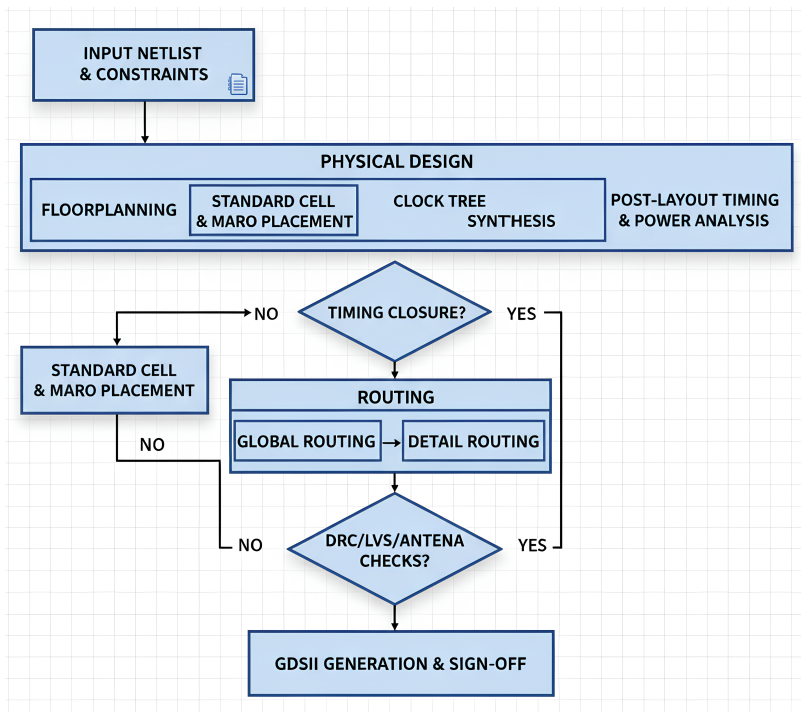


Figure 1. End to End Physical Design (PnR) Flow Implemented in ICC2

3. Pre-Floorplanning Analysis

The pre floorplanning analysis acts as an essential foundation before getting down to the actual physical design and is a check to make sure that all the inputs of the design are correct, complete, and technical and it is a check to determine the feasibility of the project before any critical layout decisions have been taken. Any mistake or variation at this point would tend to propagate and increase at subsequent stages, at worst resulting in severe congestion, timing non-closure violation or power integrity violation. Thus, the netlist, libraries and constraints need to be thoroughly verified and an initial analysis of timing behaviour should be made in order to be able to have predictable and consistent flow of downstream implementation.

3.1 Netlist and Library Validation

The first stage of pre-floorplanning phase is the verification of synthesized gate-level netlist and its correctness to the physical design environment. The netlist is what the design is supposed to be logically correct, which should have been tested, functionally, prior to physical design; it should be again verified on physical implementation to ensure that the netlist can be safely converted to physical libraries and manufacturing policies. Such checks include checking of unresolved references, consistency of instantiations of cells, pin connectivity and the absence of floating or multiple driven nets. This validation is required to prevent structural issues that can bring down the legality of placements or routing possibilities in future of the flow [2].

In order to have all the mentioned standard cell and macros in place and accurate, library validation is conducted simultaneously. Physical design is founded on abstract physical perceptions and scheduling models of standard cells and hard macros and any imposition between logical and physical instances can lead to inappropriate location, timing examination errors, or instruments collapses. Previously, the literature points out that lack of cell views, invalid pin definition or incompatible timing models are among the most common root causes of premature physical design failures [4]. The fact that the pnrblock has six hard macros and generated clocks is given special attention since the macro abstracts, pin accessibility and clock related attributes are fully supported in the physical libraries. In addition to this, multi threshold voltage cell variants must be cross-checked to ensure that all variants noted in the netlist are available and stable between time and physical perspectives. Figure 2 summarizes the composition of the gate-level netlist used for physical implementation, including standard cells, hard macros, and special cells. This breakdown provides early visibility into design scale, macro dominance, and expected routing complexity, which is critical for validating library completeness and assessing floorplanning feasibility before physical constraints are applied. This validation step implies that additional power and time based optimization is possible without introducing any undesirable functional or physical inconsistencies.

3.2 Baseline Timing Assessment

Following netlist and library validation, a baseline timing assessment is conducted to establish an initial understanding of the design's timing characteristics prior to floorplanning. This is the stage where timing analysis is performed with idealized or approximated interconnect models with the principle objective of identifying the critical paths, clock domain interactions and potential structural timing constraints. Even though interconnect parasitics are currently not physically realised, this initial analysis can be taken as a good guideline in the floorplanning decisions, particularly in architectures where interconnect delay is likely to dominate the overall timing behaviour [2].

Baseline timing analysis is particularly important in the example of the pnrblock since internal clocks are produced. Generated clocks introduce additional constraints on clock latency, uncertainty, and domain crossings, which must be well understood before clock tree synthesis and placement begin.

CELL INSTANCE INFORMATION					
Cell Instance Type	Count	% of total	Area	% of siteAreaPerSite	
TOTAL LEAF CELLS	66448	100	309159.945	100	unit:2463838
Standard cells	66442	99	60238.836	19	unit:478086
Filler cells	0	0	0.000	0	
Diode cells	0	0	0.000	0	
Hard macro cells	6	0	248921.109	80	unit:1985752
Soft macro cells	0	0	0.000	0	
Black box cells	0	0	0.000	0	
Analog block cells	0	0	0.000	0	
Pad cells	0	0	0.000	0	
Flip-chip pad cells	0	0	0.000	0	
Cover cells	0	0	0.000	0	
Flip-chip driver cells	0	0	0.000	0	
Corner pad cells	0	0	0.000	0	
Pad spacer cells	0	0	0.000	0	
Others	0	0	0.000	0	
Special cells	63	0	15.876	0	unit:126
Level shifter	0	0	0.000	0	
Isolation	0	0	0.000	0	
Switch	0	0	0.000	0	
Always on	0	0	0.000	0	
Retention	0	0	0.000	0	
Tie off	63	0	15.876	0	unit:126

Figure 2. Cell Info From Netlist

Multi-Corner Multi-Mode (MCMM) analysis is employed at this early stage of analysis to ensure timing sensitivity in representative operating conditions is measured, as is done with a single nominal corner. According to previous studies, early knowledge of MCMM will significantly reduce the risk of timing surprises and high engineering change orders (ECOs) later in the design projects [3]. The results on the baseline in time are not expected to be the objective but are instead used as the point of reference to identify the impact of the physical decisions made in floorplanning, placement and routing. The design flow can also be able to plan in advance by identifying timing sensitive regions and collections of paths and assign the routing resources and placement flexibility to the most delay sensitive regions. Figure 3 illustrates the port and pin distribution of the pnrblock. This information is used during early timing and constraint validation to ensure that all primary inputs, outputs, and clock pins are properly defined, constrained, and free of floating or unconstrained paths prior to floorplanning.

PORT AND PIN INFORMATION							
Type	Total	Input	Output	Inout	3-st	Power	Ground
Total	387877	318693	69182	0	0	66450	66448
Macro	2308	1784	522	0	0	8	6
Ports	424	36	388	0	0	0	0

Figure 3. Port and Pin Info

3.3 Design Readiness Checks

In addition to netlist validation and timing assessment, a series of design readiness checks are performed to confirm that the design is suitable for physical implementation. This verification deals with constraint completeness, clock definition correctness and design sanity. One must make sure

that all sequential paths are clocked properly, timings paths should not be free, and input and output delays must always be given [5]. Design readiness checks also verify the absence of combinational loops, improper clock gating structures, and unintended asynchronous paths, which can severely complicate both timing analysis and physical optimization. Prior work has shown that incomplete or inconsistent timing constraints, improper clock definitions, and missing I/O constraints are among the most frequent root causes of downstream timing non-closure and excessive design iterations [6]. The flow charts of the physical design process of industries always show that the unsolved constraints at this stage are the main factors of timing non-closure and long convergence loop [4]. Physically, the estimation of early congestion and connectivity analysis is analysed, to establish whether the complexity of the design and the macro distribution can be utilized together with the target utilization and the routing resources. Although the congestion analysis is later performed in greater detail, the early indicators at this point make it impossible to use impractical floorplan targets to create excessive buffering, power degradation, or routing failures [5]. The results of this set of pre-floorplanning checks include a validated netlist, consistent libraries and well-defined constraints, and a clear understanding of timing sensitivity, which put the design into the floorplanning stage. The discipline approach makes a lot of difference in predictability of physical implementation flow and offers a powerful platform to sign-off-clean performance in subsequent stages.

Operating Conditions:

Name	Process	Label	Temp	Voltage
ffg0p99v0c	1.00	(none)	0.00	0.99
ffg0p99v125c	1.00	(none)	125.00	0.99
ffg0p99vm40c	1.00	(none)	-40.00	0.99
ssg0p81v0c	1.00	(none)	0.00	0.81
ssg0p81v125c	1.00	(none)	125.00	0.81
ssg0p81vm40c	1.00	(none)	-40.00	0.81
tt0p9v25c	1.00	(none)	25.00	0.90

Figure 4. Operating Conditions Info from Library

4. Floorplanning and Power Planning

Floor planning is the initial step in the physical design process and abstract design intent is converted into the physical layout. At the 28nm technology node, routing congestion, timing convergence and power integrity are directly dependent on floorplanning choices, and therefore early planning is essential in order to obtain predictable signoff. Since modern designs are dominated by interconnect, core geometry, macro placement, and power grid topology should be well defined in order to facilitate downstream placement, clocking and routing optimization [2]. This contains a core and die configuration that is in the shape of a rectangle.

4.1 Core and Die Configuration

The pnrblock is realized with a near-square floorplan of 1:1 aspect ratio, which is selected to offer equal routing resources both horizontally and vertically. A moderate core utilization of approximately 70% is selected to maintain sufficient white space for buffer insertion, clock tree synthesis, and routing detours, which are especially important in almost all designs. Several studies emphasize that unrealistic early utilization targets and insufficient routing margin at the floorplanning stage significantly increase congestion risk and destabilize downstream timing optimization [7, 8]. There is a clear definition of separate die and core boundaries and gap should be maintained between them on each four sides. This offset allows specific space to be allocated to I/O port placement, signal escape, and physical constraints in the boundaries as well as minimizing the congestion at the core periphery. The separation of core and die in such a manner is a common industrial method in order to enhance routability and power grid resiliency at advanced nodes [5, 9].

The selection of a balanced aspect ratio and conservative use is an indication that there was a desire to support interconnect-driven optimizations without having to make too many late-stage engineering change orders. It has been demonstrated in previous work that too aggressive floorplan stage utilization targets considerably raise routing congestion and timing variation, especially when employing macro content and generated clocks in a design [2, 10]. Figure 5 shows the core and chip area parameters derived during floorplanning. These values establish the utilization target, placement boundaries, and routing resource availability, directly influencing congestion behaviour and timing convergence in subsequent implementation stages.

CORE AND CHIP AREA INFORMATION					

Core Area is :		412377.336			
Chip Area is :		416405.840			

SITE ROW INFORMATION					

Site Name	Width	Height	Total Rows	Total Tiles	Area

unit	0.14	0.90	716	3272836	412377.336

Figure 5. Core and Chip Area Info

The location of I/O ports is specified in the floorplan to ensure there is efficient signal escape and reduce congestion at the core boundary. The pnrblock port locations are placed around the core periphery so as to align with the rectangular core geometry to allow equal accessibility to routing resources both horizontally and vertically. The distribution does not cause too much clustering of ports, thus able to cause localized congestion and timing degradation of critical paths. A decent separation is allowed between core edge and I/O ports in order to allow routing of power, physical constraints of the boundary, and a clean separation between signal and power networks. The I/O placement needs to be thought of early at the stage of the floorplanning so that there are minimal routing detours and better routability in general especially in interconnect dominated designs with generated clocks [2, 5]. Figure 6 depicts the physical placement of I/O ports around the core periphery. Strategic port distribution helps reduce localized congestion, improves signal escape, and minimizes routing detours, which is especially important in interconnect-dominated designs with generated clocks.

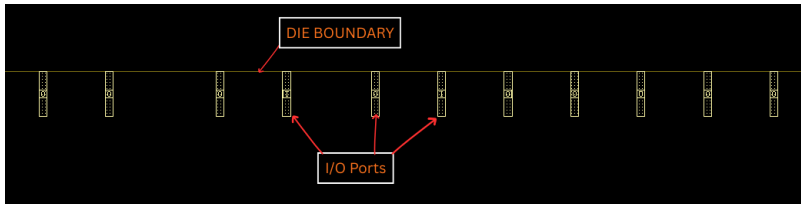


Figure 6. Port Placement in the design

4.2 Macro Placement and Halo Strategy

Macro placement is the prevailing aspect in early congestion tendencies and routing possibilities. In pnrblock the six hard macros are arranged into two different hierarchies, and the macros within the same hierarchy are positioned next to each other and are abutted along the non-pin-facing sides. This is to reduce the critical pin-to-pin routing congestion and still maintain the logical hierarchy. The rest of the macros are spread throughout the core to prevent the development of hotspots of dense congestion and to create more homogenous routing demand. All hard macros are explicitly defined by halo areas to form keep-out areas that ensure that standard cells do not be placed too close to macro boundaries. These halos provide sufficient routing access to macro pins as pin access blockage reduction and localized congestion in the detailed routing. Explicit halo strategies are highly suggested in the industrial physical design flows where macro-containing blocks are concerned because they greatly enhance routability and decrease post-route violations [4, 10]. Figure 7 illustrates the final macro placement strategy adopted for the pnrblock. Macros are positioned to preserve logical hierarchy, minimize pin-access congestion, and maintain uniform routing demand across the core, while halo regions prevent standard-cell placement near macro boundaries.

4.3 Multi-Layer Power Grid Design (M1–M9)

A multi-layer power delivery network (PDN) is designed in a manner that guarantees strong power delivery throughout the pnrblock. The PDN architecture is hierarchical where local standard-cell power delivery is performed on lower metal layers, and expansion on wider and lower-resistance power straps is made on higher metal layers. The successive metal layers are orthogonally oriented with power straps in order to enhance current spreading as well as reducing local voltage drop. This multi-layer, organized PDN system is consistent with proven physical design methodologies of nanometer-scale technologies, in which higher current density and smaller metal pitch means that one must plan carefully how resources in power routing are allocated through the routing stack [2, 4]. The PDN is embedded directly in the core area, with a dense topology based on straps to offer sufficient power coverage. This is widely used to apply sub-block implementations to larger SoCs, with global power integrity being addressed at more integration levels [5].

4.4 Early Power Integrity Considerations

Early power integrity considerations play a crucial role in floorplanning, even before detailed placement and routing are performed. In the case of pnrblock, the strategy used is a conservative PDN planning scheme to address the possible risk of IR drops due to high repeater density and clock buffering. The design minimizes the chances of late-stage power integrity violation by assigning enough routing resources to early in the flow, which will not be easy to fix without disruptive layout adjustments. In spite of the fact that detailed electromigration and dynamic IR-drop analysis are carried out at a later stage, early floorplanning choices rely on the awareness of current density and routing resource availability. Previous studies note that active planning of PDN at the floorplanning level goes a long way to enhance stability of the entire design and minimizes the chances of



Figure 7. Macro Placement in the design

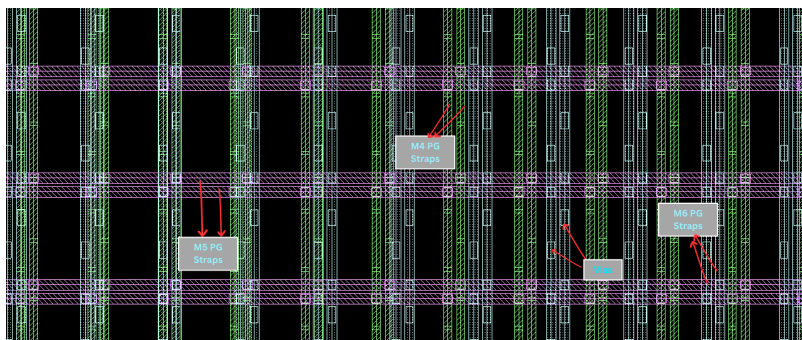


Figure 8. Representation of PDN in the design

rework of power grid during signoff [3, 4]. Figure 8 presents the multi-layer power delivery network implemented across the pnrblock. The hierarchical PDN structure ensures sufficient current distribution, reduces IR drop risk, and supports reliable operation under high switching activity, aligning with signoff-driven power integrity requirements. With the implementation flow being consistent with the signoff requirements by integrating power integrity concerns into the initial floorplan, the implementation flow ensures consistency in the timing and power convergence in later stages.

5. Placement and Optimization

Placement is also a very important meeting point in the physical implementation process where logical connectivity, physical constraints, timing goals, and power concerns start to interact in a coupled fashion. In the 28nm technology node, routability, clock feasibility and downstream optimizations effectiveness, especially in interconnect-dominated designs, can be determined by the placement quality. In the case of the pnrblock, the placement is done with a signoff-driven goal, in terms of timing robustness, congestion control and power consumption at the expense of macro constraints and conservative utilization goals. Contemporary industrial practices underscore the fact that placement is no longer a discrete geometric problem but rather one that needs a close coordination with timing, congestion and design-rule awareness in order to provide predictable closure [2, 11, 12].

5.1 Standard-Cell Placement Strategy

The standard-cell placement strategy for pnrblock is guided by the block's repeat insertion nature, macro presence, and generated clock structure. Placement is done in accordance with macro positions, halos and power grid structures that have been completely defined with the standard cells being placed only in areas that are legally routable. An initial timing-based allocation of cells is determined by a global placement phase, and then further refinement is made to achieve better wirelength, timing slack and local density. Since the design has predominantly sequential elements and buffering logic, special attention is paid to maintain logical proximity between registers, repeaters, and combinational logic to reduce the number of long interconnect segments to cause excessive RC delay and signal integrity degradation. During placement stage, threshold voltage awareness is preserved so that HVT and SVT cells can be placed without causing timing problems. The existence of generated clocks also supports the necessity of clock conscious placement, which makes sure that clock-sensitive logic is not divided between busy areas. Figure 9 shows the standard-cell placement resulting from congestion-aware and timing-driven optimization. The placement reflects controlled density, respect for macro halos, and preservation of clock and data locality, providing a stable foundation for CTS and routing. The previous industrial research indicates that the initial maintenance of logical and clock locality at the time of placement is the determinant of timing stability and minimization of unnecessary buffer insertion at the later stages [11, 12]. The resulting placement reflects a balance between timing optimization and physical regularity, providing a stable foundation for clock tree synthesis and routing.

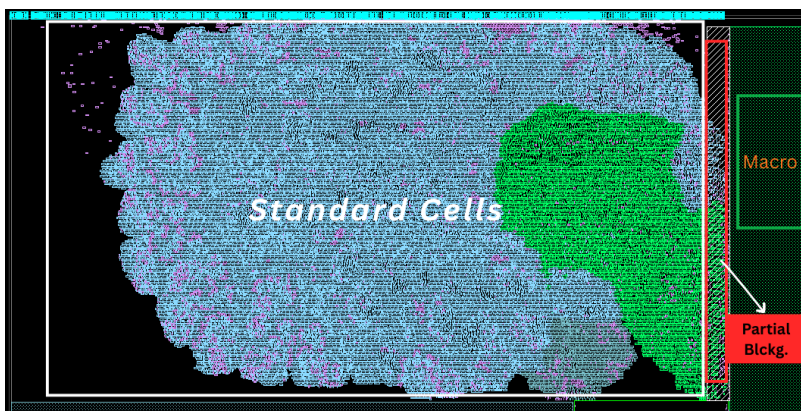


Figure 9. Representation of Standard Cell Placement in the design

5.2 Congestion and Density Management

One of the key goals of the placement is congestion management because, with repeater insertion, there is an intermediate utilization of core, macro blockages, and high interconnect activity. Placement is done with congestion information turned on, enabling the tool to predict routing demand and redistribute cells that are not on hotspots emerging. Density is also tightly managed to ensure that there is no localized over-utilization especially around macro boundaries and the interconnect corridors with high fanout. This technique will maintain an adequate amount of routing resources to both signal and clock nets to minimize the chances of detoured routing and excessive parasitic loading. Figure 10 illustrates the cell density distribution across the core. A uniform density profile with limited hotspots confirms the effectiveness of congestion-aware placement and ensures adequate routing resources for signal and clock nets. The importance of early congestion estimation is that it allows proactive correction instead of reactive correction during the routing process through the estimation of congestion. It is always demonstrated by research and industrial experience that the resulting congestion at the placement stage is not resolved, resulting in higher buffering, worse power efficiency, and inconsistent timing closure at higher nodes [2, 5, 11]. The placement strategy of pnrblock ensures that the routing complexity is minimized by maintaining a consistent density profile and keeping-out regions caused by halo effects, without compromising the flexibility of the placement strategy at any later optimization stage.

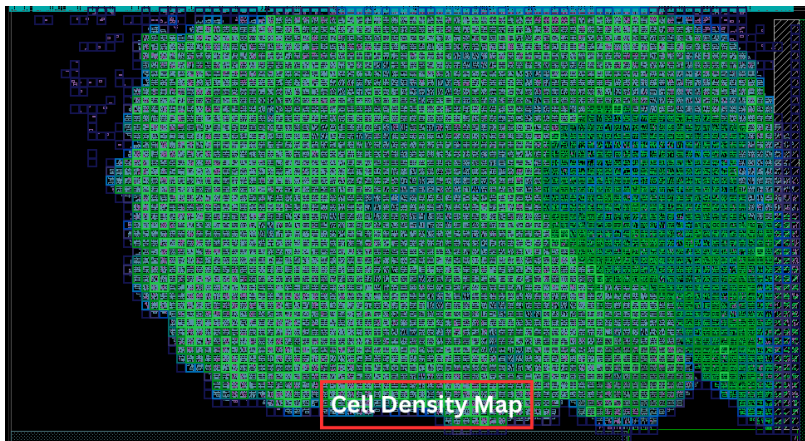


Figure 10. Representation of Cell Density in the design

5.3 Timing and DRV Optimization at Placement

During placement, timing optimization is done in parallel with density and congestion management which indicates the interdependence between physical and timing constraints at 28nm. The identification of setup-critical paths during pre-placement analysis is accorded special treatment by timing-based refinement with an aim of getting lower wirelength and better slack margins. Incorporation of early design-rule awareness placement iterations avoid configurations that cause pin access violations or routing infeasibilities. Such a design-rule focus at an early stage is a major factor that minimizes disruptive corrections in detailed routing [4, 12]. The use of Concurrent Clock and Data (CCD) optimization is used in the process of placement refinement to allow the coordination of clock and data paths, especially in areas influenced by the created clock. This method enhances convergence of timing by not over-optimizing either of the domains in isolation as is often seen in conventional single stage flows [2, 3]. Placement-stage optimization also helps to reduce the amount of risk associated with hold-times since it ensures that there is enough physical distance

and buffering capability around short paths, eliminating the need to fix hold-times at the end of the design phase. Earlier research highlights the fact that the direct incorporation of timing and design-rule issues in placement can significantly enhance predictability and decrease total convergence time in industrial PNR flows [11, 12, 13]. The optimization stage will provide a structurally sound and balanced physical basis of the pnrblock by combining timing driven placement with congestion management and early design-rule compliance. This structure supports robust clocking, efficient routing, and controlled power consumption, enabling smoother progression into clock tree synthesis and post-placement optimization while maintaining alignment with signoff objectives.

6. Clock Tree Synthesis

Clock Tree Synthesis (CTS) represents an important stage in the physical design, that acts as the critical bridge between placement and routing. At the 28nm technology node, the clock distribution network becomes the biggest consumer of dynamic power and the most impactful in attaining timing closure between several corners. The basic aim of this step is to share the clock signal at the root with all the sequential sinks and control the skew, latency and signal integrity with high strictness to guarantee the reliable synchronous functioning [5, 14].

6.1 CTS Objectives and Constraints

The pnrblock strategy revolves around the implementation of a balanced clock tree that will be healthy in different process, voltage, and temperature (PVT) conditions. The minimization of clock skew is a major concern and this maximizes the timing margin of the data paths and reduces the chance of setup and hold violations. At the same time, the insertion delay should be kept at a minimum to reduce the impact of On-Chip Variation (OCV), because the impact of local PVT variation is increased by high latency. The careful application of clock gating and optimum buffer sizing is used to ensure power efficiency by minimizing switching activity, which is a major concern in high-density 28 nm designs [2, 13]. Also, the signal integrity is given high priority by stipulating sharp transition times and use of strong shielding to avert jitter caused by crosstalk in the clock signal along long interconnect segments [15].

6.2 CCD-Based CTS Flow

In order to handle the complexities of the generated clocks and high-frequency paths in pnrblock, Concurrent Clock and Data (CCD) optimization flow is adopted. The CCD flow is capable of making simultaneous changes to both domains to produce a better timing profile as opposed to the traditional sequential methodologies which commit to the clock tree in advance optimization of data paths. This method takes advantage of valuable skew insertion, in which the implementation tool strategically introduces clock delay to the leaf cells to steal time on non-critical paths to eliminate violations on setup-critical corridors [16, 17]. This sympathetic optimization scheme provides a much better timing convergence, and less total buffers are needed to avoid data path over-design. The pnrblock can get a balanced allocation of slack and more constant timing margins across all modes by using these capabilities in Synopsys ICC2.

6.3 Clock Cell Selection and Routing

The choice of specialized clock cells and assignment of strategic metal layers is what defines the physical construction of the clock tree. Symmetric clock buffers and inverters are given priority so that the rise transitions and the fall transitions are balanced since such cells are defined by large drive and smaller sensitivity to process variations than the normal logic cells [14]. Clock signals are mostly routed on additional higher and thicker metal layers to reduce RC delay and enhance the reliability of electromigration (EM). Clock trunks are subjected to Non-Default Rules (NDR) such as double

width and double spacing constraints to minimize the resistance and coupling capacitance. Further, the active shielding with the help of VSS lines is used to ensure the distribution of long-distance clocks effectively to reduce crosstalk and ensure the stability of the signal [13, 18].

6.4 Post-CTS Timing Analysis

When the clock tree is completed, a timing analysis is performed to complete the validation of the design before the routing is actually performed in detail. This step is the passage between ideal clock mode and propagated clock mode, in which the computation of timing is made using the real delays of the synthesized tree. At this point, Multi-Corner Multi-Mode (MCMM) validation is necessary to verify that the skew and latency is kept within the allowed range at the Worst-Case corners and Best-Case corners. Figure 11 depicts the clock routing topology after CTS. Clock nets are routed using higher metal layers and non-default rules to minimize resistance, coupling, and skew, thereby supporting robust timing closure across all MCMM scenarios. The design is also checked against compliance with Design Rule Violations (DRVs) and this is to deal with max-transition and max-capacitance problems by incrementally optimizing the design. Such a strict check, which is backed up with high-quality synthesis algorithms, is to guarantee that the pnrblock has a solid clocking backbone that can support end-to-end routing and signoff goals [19, 20].

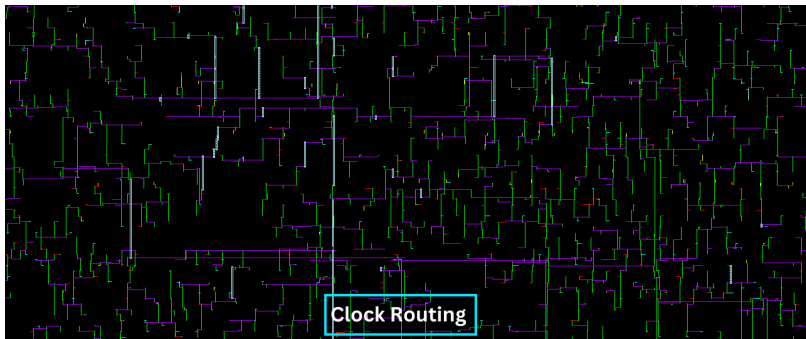


Figure 11. Clock Routing in the design

7. Routing and Signal Integrity

In the physical implementation flow, routing is the final phase where the logical connections made during floorplanning, placement, and clock tree synthesis are translated into physical metal interconnects. This stage requires a rigorous balancing, as the final geometries must achieve physical connectivity while simultaneously satisfying the timing, signal integrity, and DRCs inherent to advanced process nodes. At the 28nm technology node, routing complexity is highly enhanced by less metal pitch, high interconnect resistance, and high capacitance of the neighbouring wires. Consequently, routing has ceased to be a geometric problem but is a highly timing-constrained and signal-integrity conscious optimization problem with a decisive impact on the final quality of signoff. In the case of the pnrblock, where repeat insertion logic and generated clocks are used, and routing blockages are caused by physical design rule, routing is done with explicit timing criticality, coupling and physical design rule sensitivity to achieve stable convergence to signoff [21, 22].

7.1 Timing-Driven and SI-Aware Routing

Timing-based routing is used to make sure that important data and clock routes are given priority in the global and detailed routing stages. In this method shortest path measures are not the only factor used to make routing decisions, but timing slack sensitivity is also considered, enabling nets in

critical paths to be given preferential access to low-resistance and low-congestion routing resources. This is necessary at advanced nodes like 28nm since interconnect delay is now the most important, and routing decisions that are not optimal can render their previous placement and CTS optimization pointless. Modern routing systems use incremental delay estimation and congestion feedback to optimize routing paths dynamically as parasitics are revised [22, 23]. Besides timing awareness, Signal Integrity (SI) constraints are also directly added to the routing process. SI available routing takes into account coupling capacitance, aggressor-victim interactions and transition offset in order to reduce delay variation caused by noise and functional risk. Routing engines do not put timing sensitive nets next to high activity aggressors and use spacing or reassignment of the layer when needed to minimize the effect of coupling. Previous research on modern routing algorithms highlights that the incorporation of SI awareness in routing, as opposed to merely using post-route fixes, leads to considerably better timing stability and a reduction in disruptive Engineering Change Orders (ECOs).[22, 24].

7.2 Crosstalk and Coupling Effects

Crosstalk noise and variation in delay caused by coupling are some of the greatest causes of timing uncertainty and signal integrity degradation at the 28nm node. Capacitive coupling between neighbouring nets is becoming comparable or even greater than ground capacitance as the distance between metal spacing and length of wire increases and interconnect behaviour becomes very context-dependent. In repeat based designs like pnrblock where long buffered nets pass through congested areas, crosstalk effects have the potential to cause both functional noise glitches and large delay shifts on timing critical nets. Mitigation of these effects has been done by routing strategies which focus on controlled spacing, routing direction consistency and layer selection. Effects of aggressor alignment and simultaneous switching are taken into account in detail when performing SI analysis since the delay caused by coupling may change with relative signal transitions. Figure 12 presents the detailed routing view of the design, highlighting routing complexity in macro-adjacent and high-activity regions. Timing-driven and signal-integrity-aware routing strategies are applied to mitigate coupling effects and ensure stable post-route timing. The research in VLSI routing has demonstrated that routing with proactive coupling avoidance is more effective than routing with post-route noise fixing especially in routing with deep-submicron nodes where routing margin is not so much available [25, 23]. In turn, routing and analysis based on SI are part of the process of ensuring a reliable timing closure of the pnrblock.

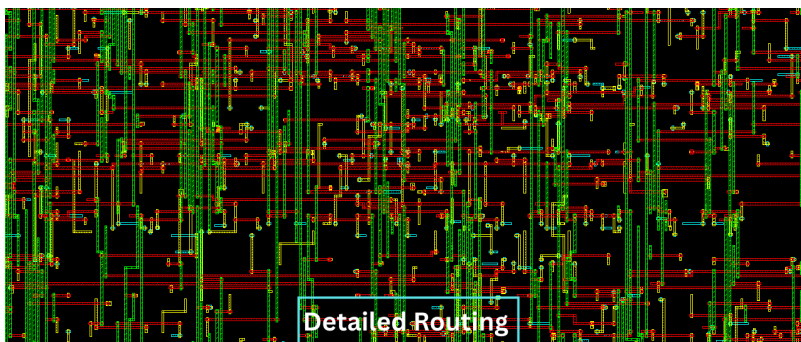


Figure 12. Representation of Detailed Routing in the design

7.3 Physical DRC Challenges During Routing

DRC is becoming more difficult when routing since the latest manufacturing rules are more complex and the signal, power, and clock systems are more tightly coupled. At 28nm, routing has to satisfy a

large number of constraints such as minimum spacing, minimum width, via enclosure, end-of-line, and metal density constraints. Breakages of these rules may be as a result of aggressive routing of timing, particularly in areas near macros, power straps and thick clock routing strips. Previous research has however established that some types of violations, including pin access conflicts and via congestion, are highly determined by the previous placement and floorplanning choices [21, 26]. This is why routing in pnrblock is an iterative optimization step instead of an execution step, and feedback loops are employed to change routing topology, routing spacing and layer allocation until timing and DRC constraints are achieved. Modern routing frameworks researches have highlighted the importance of early DRC awareness and incremental repair methods in order to have scalable routing convergence at advanced nodes [22, 24].

7.4 Iterative Optimization Strategy

Routing convergence for complex designs is achieved through an iterative optimization strategy that tightly couples routing, timing analysis, and signal integrity verification. The original routing steps are concerned with the attainment of complete connectivity and acceptable timing, which is then incrementally improved to eliminate the remaining violations of setup and hold, crosstalk, and physical design rules. In every iteration, extracted parasitics and timing models are updated which allows the identification of critical nets and congestion hotspots to be more accurate. This is especially significant to interconnect dominated designs like pnrblock where routing modifications can have unintended consequences on delay and noise behaviour. Studies of sophisticated routing algorithms point out that successful signoff is becoming more and more reliant on controlled iteration as opposed to single-pass aggressive optimization [22, 23]. The routing strategy provides a smooth transition between the design and final signoff analysis through progressive optimization of timing, SI robustness, and cleanliness of DRCs, avoiding the generation of large numbers of late-stage engineering change orders and much lateral to the industrial best practice of reliable physical implementation at the 28nm technology node [21, 24].

8. Sign-Off Verification

Sign-off verification represents the final validation phase of the physical implementation flow, ensuring that the routed layout is functionally correct, timing-clean, power-safe, and manufacturable under all specified operating conditions. The 28nm technology node has sign-off not as a one point check but rather as a multi-dimensional verification which incorporates timing closure, power integrity analysis, physical verification and design-for-manufacturability verification. Given the interconnect delay is more considered in the pnrblock, sign-off verification plays an important role in confirming that optimization stages like placement, cts, and routing that have converged toward silicon ready. Figure 13 illustrates representative routing violations identified during intermediate routing iterations. These issues are resolved through iterative optimization and rule-aware routing, leading to DRC-clean and LVS-clean signoff. The industrial methodologies place great emphasis on the fact that effective sign-off needs to be consistent in the logical, electrical, and physical realms and not a simple rule adherence [2, 12].

8.1 Timing and Global Timing Closure

Global timing closure is done by testing set up and hold constraints in all (defined) Multi-Corner Multi-Mode (MCM) cases with fully extracted post-route parasitics. At this level, clock and data paths are both propagated-clock analyzed, enabling correct evaluation of clock skew, insertion delay and uncertainty. In the case of the pnrblock, timing analysis aims at the consideration of the interconnect-induced delays added during routing do not affect the timing margins, developed in the placement and CTS phases. The coupling-aware delay shifts and local effects of congestion also

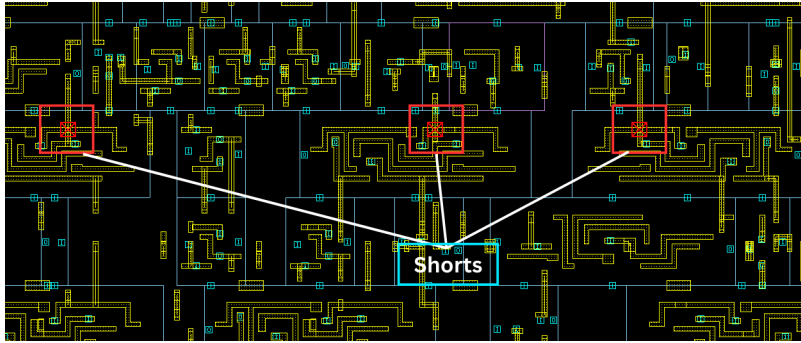


Figure 13. Representation of Shorts in the design

tend to cause residual timing violations at advanced nodes, e.g. at 28nm, which confirms the importance of post-route analysis [3, 15]. The notion of timing closure is considered to be a global property of the design and not a set of individual path fixes. Localized buffering or small scale routing refinement as incremental optimization is only used where stability is needed. Previous research points out that aggressive late-stage timing repairs may incorporate fresh infractions or diminish power productiveness and disciplined convergence is necessary to guarantee foreseeable sign-off [12, 15]. Effective timing closure across the globe thus ensures the design is able to perform the necessary requirements under all operating conditions without having to be overly pessimistic or having a narrow margin.

8.2 Power Integrity and PG DRC Verification

Power integrity verification is performed to verify the reliability of the PDN in terms of switching activity without breaching voltage drop or reliability constraints. Both dynamic and static elements of power integrity at sign-off are checked to ensure that the IR drop is within acceptable limits and that current dispersion does not cause any localized stress. Despite design-dependent detailed numerical margins, the pnrblock verification flow focuses on consistency between the topology of PDN, routing resources, and cell activity profiles determined at a higher level during the earlier stages of the verification flow.

Besides electrical check, power-grid-specific design rule checks (PG DRC) are conducted to check proper connectivity, space and enclosure of power straps, vias and rails. Restrictive manufacturing rules at 28nm, make the power structures highly sensitive to spacing and density violation especially along macros and clock routing corridors [27, 28]. As emphasized in earlier industrial techniques, routing verification has to be closely associated with PG verification since power and signal networks are competing over scarce metal resources [4, 12]. Passing of PG DRC and integrity tests ensures that design is resistant to voltage degradation and variation created during manufacturing.

8.3 Electromigration and IR-Drop Awareness in Signoff-Driven Physical Design

In addition to functional timing and power integrity checks, long term reliability considerations such as electromigration (EM) are critical for ensuring silicon robustness at the 28 nm technology node. EM effects arise due to sustained high current density in metal interconnects, particularly in clock networks, power straps, and heavily buffered signal paths. In the pnrblock implementation, EM awareness is incorporated implicitly through conservative power grid planning, hierarchical multi-layer PDN construction, and the use of wider metal routes and non-default rules on high-current nets such as clock nets. During signoff verification, current density limits are validated indirectly by ensuring compliance with foundry specified width, spacing, and via-enclosure rules, as well as by

maintaining sufficient metal utilization margins across higher routing layers. Clock trunks and major power routes are intentionally promoted to upper metal layers to reduce resistive stress and mitigate localized EM risk. While detailed vector-based EM analysis is not explicitly reported, the adopted routing topology, buffer distribution, and PDN design choices are consistent with industry signoff practices for managing EM reliability in medium-frequency, interconnect-dominated designs. This methodology ensures that power delivery and clock distribution structures remain reliable over the intended lifetime of the silicon without introducing excessive guard banding or late stage physical rework. Figure 14 Block-level power integrity view of the pnrblock illustrating relative IR-drop distribution. The contour plot reflects voltage drop variation across the core under representative switching activity and is used to flag regions that may require closer attention from a power integrity and electromigration standpoint during block-level evaluation.

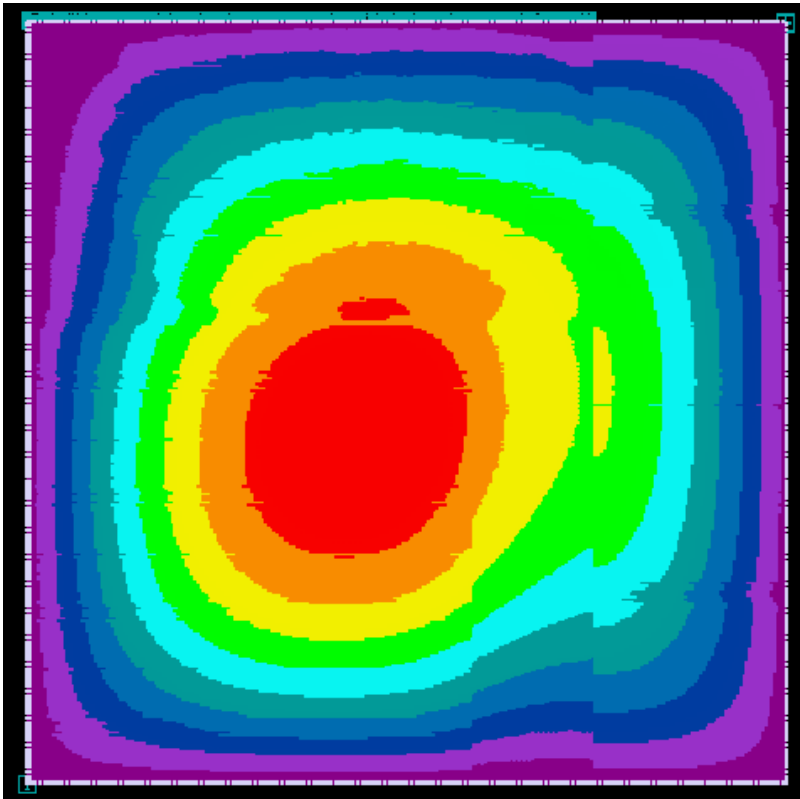


Figure 14. Power Integrity heat map for Static IR

8.4 LVS and Routing Cleanliness

Layout Versus Schematic (LVS) verification is used to verify logical correctness, by assuring that the generated physical netlist is correctly connected in the scheme that the designer intended. In the case of pnrblock, LVS checking confirms that routing optimization, buffering and antenna repair have not caused any functional connection change or added unintentional shorts or opens. LVS complexity is higher at advanced nodes as they have multi-layer routing, complicated via structures, and heavy utilization of derived connectivity thereby necessitating clean extraction to allow accurate comparison [29, 30]. Cleanliness of routing is checked by using extensive DRC closure, where all signal, clock, and power nets are checked against manufacturing requirements. Besides regular rules

of spacing and width, advanced-node routing has to meet end-of-line, via interaction, and density-related constraints that have a direct impact on yield and reliability [27, 28]. Antenna rule check is also conducted to make sure that the interconnect long segments do not store any charge during the fabrication process. Antenna mitigation measures like jumper or diode insertion are checked and proved to be correct and effective where needed [31, 32, 33]. Classical and extended research on antenna effects, charge accumulation during fabrication, and mitigation strategies such as diode and jumper insertion continue to influence modern signoff verification methodologies at advanced nodes [34, 35, 36]. A clean LVS and DRC sign-off is used to ensure that the layout has been created correctly and can be physically manufactured.

8.5 Final Design Readiness

Final design readiness is established once timing closure, power integrity, and physical verification converge without residual violations. Here, we review the design as a whole to make sure that all the sign-offs made have not brought back regressions in other areas. In the case of pnrblock, a stable MCM timing behavior, DRC-clean and LVS-clean routing, and a power delivery network meeting reliability requirements without excessive guard-banding are some of the attributes of readiness. Previous literature on the methodologies of industrial ASIC design underlines the fact that sign-off readiness cannot be achieved only by the cleanliness as reported by the tools but by the fact that there exists no weak dependencies on corner-specific optimizations or high late-stage ECOs [2, 12]. The pnrblock is brought to a state where it can be tape-out-ready, by means of disciplined convergence in timing, power, and physical verification, giving confidence that the design will work in silicon, perform well, and be manufacturable.

9. Results and Discussion

In this section, the results of the entire Place-and-Route implementation of the pnrblock with Synopsys IC Compiler II are provided. The discussion is arranged in such a way that it points out quantitative and qualitative observation at the main stages of implementation but pays more attention to the strategies of placement optimization, clocking approach, and routing conduct. The entire outcomes are based on the generated reports and layout views of ICC2 that are taken during the flow.

Table 1. Comparison between two placement stages one with High Fanout Net Synthesis Done and one with not Done

Stage	Config.	WNS (ns)	TNS (ns)	Setup Viol.	Hold Viol.	Max Tran	Max Cap	Cong. (%)	Utili. (%)
Placement	HFNS ON	0.03 (-ve)	0.64 (-ve)	0	49	0.00 met	0	0.70%	75.76
Placement	HFNS OFF	1.10 (-ve)	737.89 (-ve)	3133	0	93.07 viol.	3.63 viol.	0.70%	75.85

9.1 Metric Driven Evaluation of the PnR Flow

There are definite and quantifiable trends in the physical implementation at the successive levels of optimization. When the design is placed initially without High-Fanout Net Synthesis (HFNS), the design exhibits poor timing behaviour in the form of poor worst negative slack, high overall negative slack and extensive maximum transition and capacitance violations. The density and congestion maps in this level show that there are hotspots which are localized, especially around the macro-adjacent areas and high-fanout logic clusters, which implies that early placement by itself is

Table 2. : Results of the comparison of the timing violations between the routing stages with some switches enabled and not enabled.

Stage & Configuration	Latency		Max Skew		DRC		
	Setup	Hold	Setup	Hold	Shorts	Opens	Floating Violations
HFNS, CCD, SI Enabled	0.25 (launch) 0.08 (capture)	0.08 (launch) 0.25 (capture)	0.14	0.14	97	43	12
NO HFNS, CCD, SI Enabled	0.22 (launch) 0.09 (capture)	0.09 (launch) 0.22 (launch)	0.09	0.08	112	45	9
HFNS, NO CCD, NO SI Enabled	0.26 (launch) 0.10 (capture)	0.10 (launch) 0.26 (capture)	0.14	0.11	96	42	12
NO HFNS, NO CCD, NO SI Enabled	0.26 (launch) 0.10 (capture)	0.10 (launch) 0.26 (capture)	0.14	0.11	101	42	12

Note: All reported skew values are measured post-CTS with propagated clocks in ICC2

Table 3. Whole comparison of the all the stages in one table

Stage	Configuration	WNS setup (ns)	WNS hold (ns)	TNS setup (ns)	TNS hold (ns)	Setup Viol.	Hold Viol.	Max Tran	Max Cap	Cong. (%)	Util. (%)
Place.	HFNS ON	-0.03	-0.03	-0.64	-0.64	0	49	0	0	0.7	75.76
Place.	HFNS OFF	-1.10	0	-737.89	0	3133	0	93.07	3.63	0.7	75.85
CTS+ Route	HFNS ON, CCD OFF	-0.265	-0.03	-5.835	-0.14	95	21	0.04	0.01	0.5	75.8
CTS+ Route	HFNS ON, CCD ON	0	0	0	0	0	0	0	0	0.15	75.87
CTS+ Route	HFNS OFF, CCD ON , SI OFF	-0.20	-0.03	-6.37	-0.46	214	63	0.07	0.33	0.47	75.6
CTS+ Route	HFNS OFF, CCD OFF, SI ON	-0.07	-0.01	-2.01	-0.03	74	12	0.04	0.4	0.56	75.8

Note: Zero WNS and TNS values indicate timing closure within ICC2 reporting precision. All timing is analysed with propagated clocks and extracted parasitics.

Table 4. : Comparison table of the reference papers and the results that generated.

Metric	Literature (28nm ASICs)	This Work (rp_top)
Technology	28nm CMOS	28nm CMOS
Node		
Design Type	Processor / Generic ASIC	Repeater-intensive block
Placement Optimization	Congestion aware	HFNS vs non-HFNS
WNS after Placement (no HFNS)	Negative (reported)	-1.10 ns
WNS after Placement (HFNS)	Improved (qualitative)	-0.03 ns
CTS Technique	Conventional CTS	CCD-based CTS
Post-CTS WNS	Near-zero	0.00 ns
Global Clock Skew	<0.2 ns	~0.14 ns
Peak Routing Congestion	1–3%	0.15%
DRV Closure	Not always reported	MaxTran& Cap = 0

Note: Direct numerical comparison is limited by differences in design type and reporting granularity; the table is intended to show trend-level consistency

inadequate to interconnect-dominated designs.

With HFNS on in the placement, a significant difference in timing, congestion and density measures is seen. The high-fanout nets are broken down into buffered structures in the flow earlier resulting in shorter net lengths, better transition behavior, and more even distribution of the cell and pin density. The reports of global routing congestions indicate that HFNS minimize routing pressure as it evenly allocates fanout loads across the core. These enhancements put a better foundation of downstream CTS and routing.

Clock Tree Synthesis results further highlight the importance of integrated optimization. CTS implementation without CCD has tolerable skew control, but new hold-time violations and transition stress on clock branches. Enabling CCD during CTS in polarity causes a more balanced clock of timing slack between clock and data paths, and minimizes both setup and hold skews. Reports after CTS indicate better timing consistency all over the design and less dependency on aggressive end-of-flow solutions.

The same is the case with routing results. First-time routing with no timing-dependent and SI-insensitive switches provides connectivity, but results in the remaining maximum transition and capacitance violations. The next step is route optimization which greatly enhances timing convergence by optimizing critical net paths using extracted parasitics. All these findings show that the metrics of signoff quality at 28nm can only be attained when optimization is performed consistently at the placement, CTS, and routing stages and not at a single stage.

9.2 Implementation Challenges and Mitigation Strategies

High fanout structures in a repeat insertion block is one of the main problems that can be faced during implementation. Premature placement without HFNS results in over buffering later on, and this adds to power and congestion. This problem is addressed successfully by allowing HFNS during placement which re-distributes fanout earlier, avoiding downstream over-correction. The other major problem is encountered in CTS when clock optimization is done without considering data paths. In the absence of CCD, skew minimization will result in hold-time sensitivity and local transition violations. This is solved by the introduction of CCD, which enables valuable skew and joint clock-

data refinement, showing that current CTS cannot be approached as a series of steps but has to be addressed as a coupled optimization problem.

Routing also presents its own challenges especially in dealing with max transition and capacitance violations during realistic extraction of parasitics. The first non-timing routing step gives an idea of how connectivity is not enough at advanced nodes. The solution to the timing and signal integrity stability is incremental route optimization with proper parasitic feedback, which is vital in avoiding the unnecessary introduction of detours and DRC conflicts. Throughout the stages, the outcomes confirm an important practical point: that a large fraction of late-stage violations are not the problem of routing in itself, but an indication of decisions that were made previously in placement and CTS. The root cause approach will often be much faster to converge and less expensive to engineer.

9.3 Academic and Industry Applicability

In educational perspective, this case study offers a unique end-to-end perspective of a realistic physical design flow of 28nm with a tool of production quality. The implementation presents the learners with the real challenges of the industry, unlike simplified academic examples, which include fanout management, congestion control, clock-data interaction, and parasitic-driven timing behavior. To industrial practitioners, the research supports best practices that have been in use and also measures their effectiveness by comparing the results directly. The comparative analysis of HFNS and non-HFNS placement and CCD and non-CCD CTS represents practical evidence of the reasons why such methods are not only optimizations at the advanced level but mandatory ones. The findings are especially applicable in the case of engineers working on SoC sub-blocks where they are highly constrained in terms of power, routability, and timing margins.

10. Conclusion

This paper is a full-RTL-to-signoff physical design case study of a 28nm planar CMOS block designed using Synopsys IC Compiler II, which shows that interconnect-aware, signoff-driven optimization is the key concept to successful closure in this node, as opposed to stage-by-stage optimization. The study shows that early techniques such as High-Fanout Net Synthesis during placement and Concurrent Clock and Data optimization during clock tree synthesis are essential to control fanout, skew, and timing uncertainty, while iterative timing- and SI aware routing with extracted parasitics is required for stable convergence. One of the most notable effects is that numerous violations occurring late in the project development process can be traced back to initial architectural choices, which supports the claims that it is important to be conservative in the floorplanning, congestion-aware placement and clock-aware optimization. This work provides a clear and reproducible reference that helps to bridge the academic approach and the industry practice by recording the congestion and density patterns, and timing evolution over the entire flow. Even though the current methodology concentrates on 28nm planar technology, it can be argued that the proposed methodology has direct application to the advanced nodes, wherein the variability and interconnect supremacy further encourages automation-aided optimization and variation-conscience signoff schemes.

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