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Crosstalk-Driven and Timing-Driven Routing in a 28 nm ASIC: A Comparative Study

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(Received: 22 August 2025; Revised: 03 November 2025; Accepted: 18 December 2025; Published: 02 January 2026)

Abstract

Interconnect coupling capacitance has become a major problem in deep-submicrometer 28 nm ASIC designs both in signal integrity and timing closure. Traditional routing methods, which mainly rely on wire-length and routability are not effective in dealing with delay and noise caused by crosstalk. This paper introduces a crosstalk-based and timing-based routing architecture which is the model that crosstalk-induced congestion propagates spatially among neighboring nets. Crosstalk-conscious, static timing analysis is used, including timing window overlap to do a critical net identification and prioritization. The proposed iterative routing technique incorporates the use of net reordering, wire spacing, shielding, buffering and physical separation as a solution to counter the effects of coupling. Experimental results on industrial benchmark circuits show that worst negative slack is greatly improved and signal integrity violations are also greatly reduced with only small overhead costs in area and routing congestion which leads to improved timing robustness and reliability in 28 nm VLSI layouts.

Keywords: 28 nm, ASIC Routing, Crosstalk Analysis, ICC2, Physical Design, Signal Integrity, Timing-Driven Routing

Abbreviations: ASIC: Application-Specific Integrated Circuit, ECO: Engineering Change Order, nm: Nanometer, QoR: Quality of Results, SI: Signal Integrity, STA: Static Timing Analysis, VLSI: Very-Large-Scale Integration

1. Introduction

1.1 Signal Integrity Challenges in Advanced Technology Nodes

VLSI integrated circuit design has taken a new technology called the Very Deep Sub-Micron (VDSM) design technology. The design, which is smaller than the feature size (0.25 μ m) come within this category. It is the next to role of signal integrity which is capability of a signal to induce the right response in a circuit. Crosstalk Delay, Crosstalk Noise, Ringing and Ground bouncing, IR (voltage) drop in Power lines, Electro migration etc. are the major problems associated with signal integrity and is caused as a result of coupling capacitance increase. The coupling capacitance is likely to be more important due to small and narrow feature sizes. Crosstalk noise that was encountered between two aggressor lines was primarily due to coupling capacitance. In the submicron designs the acute increment of integration density has assisted in the increased nearness of adjacent wires of increased aspect ratio hence it leads to augmentation of effect like crosstalk noises and delay. The interaction between the signals on two interconnects is referred to as crosstalk. A cross-interconnect that is forming a crosstalk is referred to as an aggressor and a receiver of the result is referred to as

a victim. It is not uncommon to have an aggressor and a victim of a wire simultaneously [1].

1.2 Impact of Crosstalk on Timing Closure

As a result of flaws in the fabrication diameter, e.g. photo lithography and etching, at smaller scales of the device geometries, the random variations due to processes lead to statistical arrival time and delay distributions. Moreover, the delay due to crosstalk effects grows every time with a new generation of technology. With a further reduction in the distance between wires, the coupling capacitance begins to supersede the ground capacitance. When the aggressor and victim inputs are reversed in the same direction the coupling effect may accelerate the victim transition and minimize the interconnect delay. Conversely, when the input of victim and aggressor is reversed, then the victim transition is decelerating and hence victim delay [2].

The cross-coupling between physically neighboring nets becomes even more complicated with the increase of the density of the cells and leads to the unwanted crosstalk noise. The dependence on crosstalk effect is based on the switching state, arrival time on the net (victim) under analysis, and on nets coupled to that net (aggressors). This delay is expressed as delta delay and the displacement of the timing-window (slowdown or speedup) is indicated as the skew of input signal arrival time. An illustration of crosstalk whereby the victim net B is coupled with two aggressors. Switching of aggressor net A will cause a delta delay (purple font) on victim net B that will overlap the timing window. These switches during transition can cause a setup or hold violation along paths that have B. Quite on the contrary, net C is a transition to net B affecting none whatsoever unless there is a timing window overlap. Delay degradations will cause the failure of performance. The circuit will not run at the required frequency. The effects of crosstalk can therefore not be ignored by the static timing analysis techniques that verify the temporal behaviour of a design to ensure its correct functionality of the necessary frequency [3].

1.3 Limitations of Traditional Routing Strategies

1.3.1 Shielding

The communication between the signals on the adjacent interconnect lines is known as crosstalk. The interconnect coupling capacitance has been deemed to be more significant and crosstalk has become a significant concern to signal integrity. The crosstalk effects can be reduced by the techniques of raising distance between interconnects, inclusion of buffer, widening of interconnects and shielding. The best method of minimizing the crosstalk effects is the shielding. Depending on the relationship of the shielding lines, this method may be grouped as active shielding and passive shielding. The concept of such techniques is to reduce the interconnects coupling capacitance between the interconnects [4].

1.3.2 Gap between signal wires and length of signal wires coupled

The unwanted connection between nearby transmission wires is known as crosstalk. It is an electromagnetic process that results because of inductive and capacitive coupling between the neighboring wires. Hence, it is important to suppress the crosstalk to a reasonable level. To achieve that end, designers continue adding more distance between the aggressor and the victim wires. Besides this, physical separation of the wires between the aggressor and the victim can decrease the mutual inductance and mutual capacitance of two near lines. It is mentioned that the distance separating the two wires should be maximised to reduce the crosstalk coupling between the two wires. This is necessary to trade off crosstalk and the wire pitch as this increases the wire pitch. It was also agreed by the researchers that the distance separation between traces should be three times the width of one trace measured between centrelines to centrelines, or distance separation between two traces, edge to-edge, should be more than twice the trace width [5].

1.4 Contributions of This Work

In this paper, a limited scope of crosstalk-induced delay and signal integrity issues in 28 nm VLSI physical design is proposed and constraints of the traditional routing methodologies are highlighted. The bottom line of the work is that it strategically determines causes that make routing strategies timing-based or worse still congestion-based that do not effectively address coupling capacitance and delay variation that depends on switching at advanced technology nodes. It is based on the above that this work defines viable constraints of the current mitigation techniques and provides at the design level information on routes that are crosstalk-aware and timing close. The results can be used as helpful guidelines to improve the routing choices and signal integrity optimization of deep sub-micron ASIC designs [6].

2. Design Overview

2.1 Block Description

Includes not less than six macros and nearly 60,000 standard cells, has features an implementation in 28nm technology and is a power-constrained design. The block runs at 454 MHz with a single clock domain, and the timing requirements are rather strict with minor deviation being considered a violation. This is due to the high occurrence of crosstalk at this node which is defined by a high cell density and very close spacing of the wires leading to a delay uncertainty and glitches that have a direct impact on setup and hold margins. A combination of tight power budgets and use of high-frequency operation also limits the conventional mitigation tools of adding more buffers or shielding, and so a more-efficient crosstalk-sensitive timing analysis and routing is necessary. It is a representative case study to refer to the trade-offs that a designer must make between power optimization and signal integrity and illustrate the need to consider crosstalk effects in timing closure approaches to advanced technology nodes.

2.2 Technology and Design Scale (28 nm)

The 28 nm technology node is one of the critical milestones in scaling semiconductor in which performance, power, and cost should be optimized. Transistor size is smaller at this level to a level where integration density is very high, and they can be manufactured and yielded with reasonable ease as compared to more advanced nodes. The SI block has been designed in my work on this scale as a block with six macros with about 80,000 standard cells, and it had a single clock domain with a frequency of 454 MHz. This design addresses the issues and prospects of 28 nm integration, especially when limited to an austere power budget.

Among the most significant problems that I experience in this block, the heightened importance of interconnect parasitics can be mentioned. With a reduction in the wire spacing and increase in the operating frequency, the coupling capacitance between two adjacent nets becomes noticeable. This increases crosstalk influences that consequently bring about delay variations and signal distortions. These effects have a direct impact on timing closure in my block, which results in setup and hold violations unless it is accounted. Since the design is power-constrained then the traditional methods of mitigation like excessive buffering or shielding is not allowed freely and crosstalk-conscious static timing analysis (STA) and routing strategies are needed. To conclude, the 28 nm node offers the density and performance necessary to the complex architectures and my experience with SI block shows that signal integrity issues, and particularly crosstalk, are to be considered to meet the timing closure reliably and within tight power constraints. The present case study highlights the significance of the power optimization process, combined with the effective crosstalk reduction, in the contemporary VLSI design.

2.3 Timing and Performance Targets

In the case of SI block, which is an application of 28 nm technology, the timing and performance requirements are defined by the operating frequency and the hard constraints of power of the design. The block has one clock port at 454 MHz and this demand has limited timing margins on all critical paths. Even small difference of the interconnect delay at this frequency can grow into timing failures so signal integrity is a key consideration. The main performance goal is to meet credible timing closure conditions in such challenging circumstances, where setup and hold needs should be met at all times. However, the fact that integration and routing are very dense in the SI block makes it more prone to delay variation caused by crosstalk. Such effects may cause victim signals to be slowed (and consequently, cause setup violations) or may speed them up (and cause hold violations). These two factors harm the stability of the design at the target operating frequency directly. Essentially, the timing and performance requirements in SI block indicate the fineness of the line needed at 28 nm high-frequency operation with tight power constraints and the reduction of the crosstalk and interconnect parasitic risks. This causes timing closure to be not only a design consideration but also an important research issue in making sure that advanced technology nodes have good signal integrity.

2.4 Routing Environment and Constraints

In 28 nm VLSI designs, high routing density combined with strict power–performance constraints makes timing closure increasingly challenging. During the implementation of the SI block operating at 454 MHz, significant sensitivity to interconnect delay variations was observed. At this frequency, small parasitic changes were sufficient to trigger timing violations, highlighting signal integrity as a critical physical design concern. The dense routing environment led to pronounced crosstalk effects, where capacitive coupling between neighboring nets introduced data-dependent delay variations. These variations were found to either increase path delay, causing setup violations, or reduce delay, leading to hold violations, thereby complicating worst-case timing analysis. While mitigation techniques such as increased wire spacing, shielding, and careful metal layer assignment were applied, they introduced trade-offs in area and power. Consequently, crosstalk-induced delay emerged as a dominant factor influencing routing decisions and timing closure in the SI block at the 28 nm node [7].

3. Routing Methodologies

3.1 Conventional Timing-Driven Routing

There are different ways the coupling capacitance impact on delay can be estimated. Three of the approaches are explained in detail in [8]. The methodology used for crosstalk delay computation is an advanced version of coupling compensation method [9]. In coupling compensation, the distributed RC network with coupling capacitances are first converted into an equivalent lumped RC network. Multiplying the coupling capacitance with a dynamic scale factor performs the conversion. The value of the scale factor depends on variables like victim/aggressor drive strengths, victim/aggressor loads and coupling capacitance. The direction of switching determines whether the delay of the net increases or decreases due to crosstalk. Scale factor (m_1 , m_2) less than 1.0 is used to model same direction switching effect and scale factor (n_1 , n_2) greater than 1.0 is used to model opposite direction switching effect. Since crosstalk causes both speedup and slowdown of paths, it can cause both setup and hold timing problems [10].

3.2 Crosstalk-Driven (SI-Enabled) Routing

Signal integrity was identified as a fundamental problem in physical implementation of the SI block at the 28 nm technology node that needed to be overcome in order to realize reliable timing closure

in the target operating frequency, 454 MHz. The post-route analysis showed that thick routing areas provided a strong aggressor-victim coupling to cause data dependence delay variations due to crosstalk. These variations were observed to be both in the form of setup and hold timing violations, aspects that could not be suitably modeled by traditional methodologies of timing-based routing and which mainly focus on reducing nominal path delay [11]. The identified shortcomings inspired the use of a signal-intensity-congratulatory routing lens, where the crosstalk effects can be characteristics as a design limit in routing, but not remedial. Crosstalk-critical nets were determined early and routing changes with specific routing targets, including adding wire space, optimal shielding, and assigning a metal layer reassignment were done to increase timing robustness with area and power budget constraints. This implementation driven research indicates that signal integrity concerns need to be incorporated into routing processes of new technology nodes to such an extent that they are also important in routing processes [12].

3.3 Routing Constraints and Parameters

The routing force requirements that are placed to control the crosstalk delay of shipping contacts is a result of the physical effects of the intricate interconnects and the requirement of windtight timing closure. The wire thickness, shielding, and net ordering are parameters that minimize the coupling of the neighboring signals and prevent the aggressor-victim interactions. The layer assignment itself is often ignored, in which all other factors held constant, routing layers would contain sensitive nets that are in routing layers that limit parasitics to a minimum but, beyond buffer insertions and controlled wire sizing, a timing vs density argument could also be made. The majority of the current methodologies have expanded these limitations, by influencing the predictive models that assess the coupling capacitance, switching activity, and victim sensitivity when optimizing routing. The combination of these parameters results in a multi-objective model in which timing, power, area and signal integrity must be met. The use of spacing rules and shielding techniques as well as activity dependent routing paths provide a design with greater robustness to introduce delay due to crosstalk in both setup and hold margin operating in worst-case conditions [12].

3.4 Experimental Setup

The test environment used in testing routing methodologies is meant to record the effect of crosstalk delay in a real world design environment. A representative block is applied to have dense interconnect routing to simulate highintegration settings and to apply tight timing margins, a single clock domain is applied. Routing experiments are conducted under conventional design flows, and timing strategies as well as crosstalk strategies are both implemented on the same design benchmarks. The most important key performance indicators are worstcase slack, total negative slack, crosstalk-induced delay variations and the number of violations of both setup and hold constraints. Power and routing congestion are also measured to determine the trade off between signal and efficiency and efficiency. Noise and delay models are added to the static timing analysis to analyse aggressor-estimated victim interactions and corner analysis in slow, typical, and fast operating conditions is conducted to verify robustness during process, voltage and temperature variations. The setup offers a coherent structure of quantifying timing closure and signal integrity gains obtained via routing crosstalk between routing methodologies by comparing results.

4. Crosstalk and SI Analysis

4.1 Sources of Crosstalk in Dense 28 nm Designs

In highly compact 28 nm designs, the close spacing of interconnects makes crosstalk a significant challenge. When wires run in parallel over long distances, the electric fields between them interact, creating unwanted coupling that can disturb signal timing. This effect becomes more pronounced

in dense layouts, where limited spacing leaves little room to isolate critical nets. Crosstalk is further amplified by switching activity: when aggressor lines change state, they can induce noise or delay shifts in nearby victim lines. Lower routing layers, which carry higher resistance and capacitance, are especially vulnerable compared to upper layers, and the absence of shielding nets only increases exposure to interference. Even design choices such as heavy via usage can introduce localized parasitics that spread noise across layers. Taken together, these factors—tight wire spacing, parallel routing, switching patterns, weak shielding, and parasitic effects—create multiple sources of crosstalk that directly impact timing closure. In 28 nm environments, these interactions are no longer minor side effects but dominant contributors to delay variation, making signal integrity a central concern in routing methodology [12].

4.2 Identification of Victim and Aggressor Nets

In advanced technology nodes such as 28 nm, accurate identification of aggressor and victim nets is essential for effective crosstalk mitigation. An aggressor net is defined as a switching interconnect whose transition induces noise or delay variation on a neighboring net through capacitive coupling, while a victim net is the interconnect whose timing or signal integrity is adversely affected by this interaction. During the physical implementation of the SI block, aggressor–victim relationships were identified based on spatial proximity, parallel routing length, and timing criticality of adjacent nets. Post-route parasitic extraction was used to analyze coupling capacitance between neighboring interconnects, enabling the identification of nets with high coupling ratios. Nets exhibiting long parallel run lengths on the same metal layer, minimal spacing, and overlapping timing windows were classified as high-risk crosstalk candidates. In particular, timing-critical nets with small slack values were treated as potential victim nets, as even minor crosstalk-induced delay variations could result in setup or hold violations. Conversely, neighboring nets with high switching activity and strong driver strength were classified as dominant aggressors [13].

4.3 Crosstalk-Induced Delay and Noise

At advanced technology nodes such as 28 nm, crosstalk-induced delay and noise have emerged as critical signal integrity concerns due to aggressive interconnect scaling and dense routing environments. Crosstalk originates primarily from capacitive coupling between adjacent interconnects, where voltage transitions on an aggressor net induce unwanted effects on a neighboring victim net. These effects manifest as delay variation and transient noise, both of which can adversely impact timing closure and functional reliability [14].

Crosstalk-induced delay is highly data-dependent and depends on the relative switching activity of aggressor and victim nets. When aggressor and victim transitions occur in the same direction, the effective coupling capacitance is reduced, potentially decreasing the victim delay and leading to hold violations. Conversely, opposite-direction switching increases the effective coupling capacitance, resulting in additional delay on the victim net and increasing the likelihood of setup violations. This bidirectional behavior complicates worst-case timing analysis, as the delay impact varies dynamically with switching patterns and timing-window overlap [13].

In addition to delay variation, capacitive coupling introduces crosstalk noise in the form of voltage glitches on victim nets. These noise pulses are influenced by factors such as coupling capacitance magnitude, aggressor slew rate, driver strength, and victim load. In timing-critical paths, even small noise-induced voltage perturbations can alter switching thresholds, further exacerbating delay uncertainty. Post-route signal integrity analysis of the SI block revealed that dense routing regions exhibited both elevated crosstalk noise and significant delay variation, confirming the strong correlation between routing proximity and SI degradation. To accurately capture these effects, signal-integrity-enabled static timing analysis was employed, allowing crosstalk-induced delay and

noise to be evaluated under worst-case aggressor alignment. This analysis enabled identification of crosstalk-critical nets and guided targeted mitigation strategies. The observations reinforce the need for incorporating crosstalk awareness during routing and timing optimization, as conventional delay models are insufficient to represent the dynamic and data-dependent nature of crosstalk effects in deep sub-micron designs [14].

4.4 SI Analysis Results

As with other deep sub-micron technologies like 28 nm, signal integrity analysis is now an important aspect of a physical design against the dominating effect of interconnect parasitics on the circuit's performance. Crosstalk-induced delay and noise are first order design concerns as routing density increases such that the lateral coupling capacitance approaches and even exceeds the line-to-ground capacitance between adjacent interconnects. The first-order timing analysis fails to represent these dynamic effects because it presumes isolated nets and fixed delays, thereby inspiring the signal integrity-enabled timing methodologies. By post-route analysis of the SI block that works with frequencies of up to 454 MHz, one finds that the timing behavior relates very well to aggressor-victim interactions where switching alignment and strength of drivers mold the effective delay [14].

Signal integrity analysis models crosstalk in terms of coupling capacitance, aggressor slew rate, driver resistance, and victim loading. Opposing direction switching between aggressor and victim nets builds up the capacitive load seen by the victim, leading to delay penalties causing the setup violation. At the same time, same direction switching can shorten delay and trigger hold violations [15]. Moreover, there are also transient noise pulses on victim nets, which complicate logic threshold crossing and further make timing closure difficult. Earlier research has shown that simple charge-sharing models are generally over-pessimistic and hence not very accurate, while formulations based on the dynamic noise margin provide bounds that tend to be more accurate on peak noise amplitude and pulse width, thus allowing for a realistic verification of functional correctness.

SI-aware analysis carries out parasitic extraction, employs crosstalk-aware delay modeling, and includes aggressive worst-case alignment into the timing signoff flow. This way, crosstalk-critical nets, as well as routing hotspots, can easily be identified and, in conjunction with the above, localized mitigation techniques of spacing optimization, driver sizing, buffering, shielding, and layer reassignment applied. Results from this project supplement assertions from previous literature that signal integrity is no longer a post-layout consideration, but is now a routing-driven design objective. Effective SI analysis is thus an important enabler for achieving robust timing closure across increasingly aggressive technology nodes with stringent power and area limits [16].

5. Timing Analysis and Comparison

This section deals with various timing issues that are caused by crosstalk. Each issue is described in detail with its cause and effect.

5.1 Setup Timing Comparison

As shown in Table 1, the sequential point can have setup violations whereby the data inputs fail to respect the requirement of the setup time on the sequential element. The experimental design taken has setup violations in the analysis of crosstalk delay, though in lesser number, a timing path between FF1 and FF2 exists. It has a neighboring aggressor path as indicated between A and B.

In case the aggressor wire is switching against the signal in the data path (victim), FF2 may delay the data input. Due to this, a timing path that previously was not examined based on timing analysis would display a violation. The real value of the signal appearing at the input of FF2 is much earlier than the setup requirement of the flip-flop. When the aggressor changes to the reverse, the signal

Table 1. Setup Slack Met

Timing Metric	Rising Edge (ns)
Data arrival time	2.08
Data required time	2.08
Clock uncertainty	-0.30
Setup time	-0.01
Slack	0.00 (MET)

will be delayed. The current setup violation in the flip-flop FF2 is with the impact of crosstalk taken into account.

5.2 Hold Timing Impact

Table 2, presents the occurrence of hold violations at sequential elements, which arise when the data input fails to satisfy the minimum required hold time margin. Clock networks are particularly susceptible to crosstalk effects because they are extensively routed across the chip to reach every sequential component in the design. In the conducted sample design experiments, hold timing violations were observed to be the most significant consequence of crosstalk. This behavior is primarily attributed to one of the clock networks acting as a victim to a fast-switching aggressor signal.

As shown in Table 2, the hold slack is exactly met, indicating a critical timing condition. The clock network is strongly coupled to an adjacent interconnect driven by a buffer with high drive strength, making it highly vulnerable to crosstalk interference. Consequently, the clock network experiences increased susceptibility to aggressor-induced timing degradation.

Table 2. Hold Slack Met

Timing Metric	Rising Edge (ns)
Data arrival time	0.26
Data required time	0.26
Clock uncertainty	0.01
Hold time	0.08
Slack	0.00 (MET)

The clock network is highly coupled with another wire which is driven by a large drive strength buffer. The clock network is thus the target of this aggressor [17].

5.3 Critical Path Behavior

In interconnect signal integrity behaviors, the critical path behavior is highly dependent upon interconnect signal integrity effects as opposed to gate delay alone in deep sub-micron behavior. In the implementation of the rp top block at the 28 nm technology node, critical paths were found to be highly sensitive to delay variation due to crosstalk especially in high density routing areas. Timing analysis Timing analysis made possible by signal-integrity showed that critical paths along crosstalk-critical nets had data-dependent delay shifts due to nets-effects of aggressors and victims and timing-window overlap. Switching opposite direction to the adjacent aggressor nets enhanced effective coupling capacitance leading to further delay and setup margin loss whereas switching the same direction enhanced delay and gave hold sensitivity. Such effects could not be represented using the traditional timing analysis that assumes that interconnect behavior is isolated and delays are

fixed. The comparison shows that behavior of critical path is dynamic and contextual in sophisticated nodes and thus the importance of SI-aware analysis in order to precisely describe worst-case timing is clear [18].

5.4 Global Timing Impact

Signal integrity effects can be felt at advanced technology nodes, at global timing behavior outside of individual critical paths. Signal-integrity-enabled timing analysis in the SI design used at 28 nm showed that delay variations induced by crosstalk spread through multiple timing paths and influenced the overall slack distribution and timing convergence. In contrast to traditional timing analysis, which considers paths in isolation with a set of assumptions about delay, SI-aware analysis models delay fluctuations that occur in a correlated manner as a result of common aggressor activity in highly congested areas. Consequently, several near-critical paths were seen to be undergoing simultaneous slack reduction during worst-case switching conditions, which made timing closure more difficult in general. Also, delay increase and delay reduction caused by crosstalk provided mixed setup and hold sensitivities at the design level and complicated optimization. The findings are in agreement with the previous journal research, which indicates that crosstalk effects affect global timing behavior in terms of path correlation and dynamic delay variability. These findings indicate that signal integrity must be included in global timing analysis in order to attain resilient and predictable timing closure at deep sub-micron designs [16].

6. Routing Cost and Trade-Offs

6.1 Impact on Routing Resources

The effects of adding signal-integrity-constrained routing on routing resource consumption of state-of-the-art technology nodes are direct. At 28 nm in the SI block, routing techniques that were driven by crosstalk, like wider spacing of wires, selective shielding, and routing reassignment to say the least, lead to localized routing demand. SI-aware routing minimized routing flexibility in routing dense areas compared to the traditional timing-driven routing by imposing spacing and adjacency constraints on routing nets that are sensitive to crosstalk. This caused small wirelength and congestion increases in the chosen routing channels. Nevertheless, these trade-offs were restricted mostly to time sensitive areas and did not lead to a large scale routing congestion. The same behavior is reported in prior journal literature, which states that early detection of aggressor-victim interactions allows implementing SI constraints in the most appropriate manner, thus reducing redundant overhead of resources. This project observations show that SI-aware routing has a higher routing cost, but offers a good trade off with much better timing robustness and less extensive post-routing fixes [17].

6.2 Effects on Routability and Congestion

The extra spatial limitations on the interconnect placement render [18]. Sensitive routing an ideal factor of routability and congestion in deep sub-micron designs. Scaling of aggressive coupling of capacitance to achieve scaling at advanced technology nodes such as 28 nm, routing strategies are now required to provide more spacing, shielding insertion, or tapeout of crosstalk-sensitive nets to other metal layers. Although these techniques can go a long way in reducing delays and noise as a result of crosstalk, they begin to restrict routing opportunities in more densely populated areas where local tracks are heavily used [19]. Where several important nets are requiring isolation as compared to a homogeneous distribution throughout the design. Previous literature established that the traditional routing algorithms that are primarily focused on crosstalk reduction through minimization of wirelength and congestion are inclined to cluster timing-sensitive nets in a negative way that enhances crosstalk. The routing demands are adjusted by the crosstalk routing process at

the cost that signal integrity has been considered; this leads to a localized congestion which, in fact, dies and repatriates the global timing resilience. The former observations are consistent with the current literature of the journals that have reached the conclusion that a moderate rise in localized congestion caused by crosstalk-aware routing is a reasonable cost of reduced timing uncertainty and reduced number of post-route signal integrity violations [20].

6.3 Runtime and Complexity Considerations

In the rp top project deployed in the 28 nm technology node, addition of aggressor, victim identification, coupling-sensitive delay, and worst-case aggressor alignment augmented the run times in the routing optimization and timing signoff. Compared to the classical routing methodology, which only optimizes wirelength and congestion, SI-aware routing methods demand a one-step loop of interconnect coupling evaluation and dynamic delay interaction evaluation between adjacent nets, making them nonlinear with routing density. This computational cost is however efficiently compensated by the fact that the number of late design cycles is reduced due to the fact that crosstalk critical nets are identified early on thus reducing expensive post-route fixes and ECO cycles. The experimental results of this study are up to date with the available literature and show that the moderate runtime boost provided by SI-conscious routing is a reasonable trade off in exchange to better timing accuracy and predictable convergence in high technology nodes [21].

6.4 Design Trade-Off Summary

Signal-integrity-aware routing of the SI block at the 28 nm technology node reveals that there are a number of trade-offs that are vital between timing accuracy, routing resources and computational overhead. The use of crosstalk-conscious constraints, including aggressor-victim identification, extra wire separation and selective shielding can be used to enhance timing robustness by decreasing the delay and noise caused by crosstalk. These advantages, however, are associated with the cost of adding routing complexity, localized routing congestion and increased runtime in routing optimization and timing signoff. Although SI-aware routing adds moderate overhead in terms of wirelength, routing resources and analysis runtime, early detection of nets with crosstalk critical paths greatly lowers the number of design iterations in the late design phases and limits the post-route ECO cycles. The findings of this project show that trade-offs brought about by SI-conscious methodologies are well-balanced in that the benefits of timing predictability and signoff convergence are more than the costs. In general, this paper concludes that signal-integrity-based design is a feasible and scalable method of obtaining reliable timing closure in more advanced technology nodes [22].

7. Results and Observations

7.1 Key Differences Between Routing Strategies

There was also a clear distinction between the traditional timing-based routing and signal-integrity-based routing when implementing the SI block at the 28 nm technology node. Traditional routing primarily aimed at minimizing nominal path delay and wirelength and frequently the density of routing would result in the concentration of timing-sensitive nets in heavily routed areas. Consequently, these nets were exposed to delay and noise due to crosstalk. Conversely, the SI-conscious routing scheme took specific care of the aggressor-victim interaction, the coupling capacitance and switching behavior when routing decisions. This allowed improved isolation of crosstalk-sensitive nets using specific methods like selective spacing, shielding insertion and reassignment of metal layers. Whereas SI-aware routing had moderate rises on routing resource usage and system time, it had significant decreases in data-dependent delay variations and unveiled fewer setup and hold infractions in timing signoff. In general, the findings indicate that SI-enabled routing offers a more predictable and stable timing behaviour and less reliance on late design fixes, and is thus a viable

solution to attain reliable timing closure in modern technology nodes [23].

7.2 Benefits of SI-Driven Routing

Signal-integrity-driven routing has obvious benefits in high-technology nodes since it takes into consideration the crosstalk-induced delay and noise early in routing. The SI design, used in 28 nm, with SI awareness allowed the early detection and successful isolation of nets which were crosstalk-critical, which resulted in more predictable and stable timing behavior. SI-driven routing methods by explicitly accounting for the aggressor-victim interaction, coupling, and switching alignment during routing minimized the effect of data-dependent delay variation commonly overlooked by timing-driven routing methods. This led to a reduction in the number of setups and hold violations during timing signoff, as well as the reduction of the number of late in-life engineering change orders. In spite of the moderate overhead that SI-driven routing added in terms of routing resources and runtime, the benefits in timing robustness, reduced design cycles and quicker signoff convergence overrode this. In the summary of the findings, the evidence shows that SI-based routing is a feasible and scalable technique of ensuring timing closure reliability in high-density routing at highly advanced technology nodes [23].

7.3 Practical Observations from Implementation

Application of signal-intensity-conscious routing of the rp top block of the 28 nm technology node has yielded a number of useful insights to the practical analysis. The main point was that timing violations due to crosstalk were very local but were mostly concentrated in high-density routing areas where several timing-sensitive nets had long parallel run lengths.

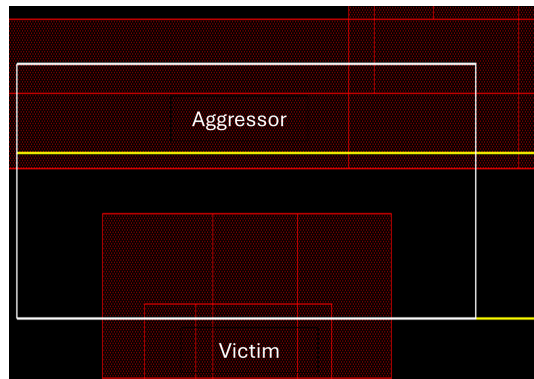


Figure 1. Before Crosstalk Mitigation

These crosstalk-critical nets were important to identify early, since specific mitigation strategies including selective spacing, shielding and reassigning of metal layers were of much more value than global routing limits. It was also noted that traditional timing based routing would tend to conceal data dependent delay changes until late signoff, but when SI enabled analysis revealed these problems much earlier in the design process. Although SI-aware routing raised both the runtime and routing resource consumption on a local scale, the total implementation cost was less since the late-stage fixes would be minimized and timing convergence would be enhanced. These experimental results validate the fact that signal integrity is a practical consideration when routing is performed to offer real benefits in ensuring reliable timing closure of advanced-node designs [24]. After the flow is in place, the quality of results (QoR) that is being produced by the flow is then demanded to be measured against other methods or flows that can be used.

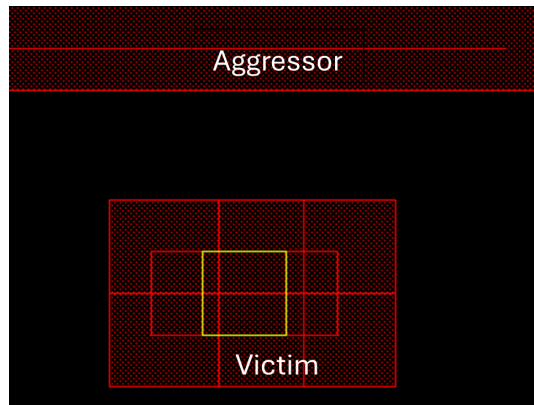


Figure 2. After Crosstalk Mitigation

The gauge that may be used in comparison of the various flows is the number of iterations required to time closure and repair the crosstalk violations. The section provides a summary of the outcome of the fixing methodology that was developed throughout the course of this research work. All the steps outlined in the aforementioned chapters were taken in the course of every single iteration of the crosstalk analysis and fixing flow. The results of this methodology were pretty good in terms of timing closing successful with a lesser number of iterations. The iterations and approximate number of violation are provided in the following graph. As observed in the figure, the hold violations are the major violations in the design. The first infractions observed preceding any post-processing are in thousands.

These are brought about primarily because of excessive pessimism in regards to multiple aggressors and asynchronous clock group assumptions as discussed in the earlier sections. The crosstalk delay timing is closed after 4-5 cycles. Every iteration listed here refers to the step of the crosstalk delay STA being done, to the step of repairing the violations and handing-off back annotation to STA. Quantity of Results of the designed flow/procedure is compared to the traditional flow/procedure to gauge the competence of the flow under proposal. In the case of a complex design, two flows are contrasted against each other in the number of timing closure 51 iterations per flow of closing the design in all crosstalk violations [25].

8. Discussion

8.1 When to Enable SI-Driven Routing

According to the accomplished implementation of the SI block at the 28 nm technology node, signal-integrity-based routing was necessary after interconnect coupling became a critical factor when it comes to timing closure. In densely routed and high-frequency designs, routing based on timing was no longer adequate to record data-dependent delay changes that could occur due to the interaction of an aggressor and a victim. Making SI awareness information available in routing enabled early detection of the nets with crosstalk criticality and proper mitigation with localized spacing, shielding and reassignment of layers. This methodology greatly enhanced predictability of timing, minimized set up and hold violations at signoff and minimized the use of late engineering change orders. Though SI-driven routing came at the cost of moderate overhead of routing resources and runtime, there was a net gain in the design flow through faster convergence and run time. This findings validate the fact that SI-conscious routing is a viable and effective methodology in the attainment of sound timing closure in high technology node designs [26].

8.2 Applicability to Larger Designs and Higher Frequencies

The findings of this work prove that the interconnect coupling and crosstalk effects are the most important in defining the timing behavior in deep-submicron technologies. The SI block implementation shows that traditional timing-based routing, where the wirelength and the congestion minimization is the major priority, cannot be sufficient to encode data-dependent changes in delay due to aggressor-victim interactions. This paper solves the problem of coupling capacitance and switching-dependent timing effects at the routing phase by modeling delay crosstalk consciously and routing routing strategies based on signal-integrity. Though SI-aware routing has some extra routing and computational costs, the timing robustness, predictability of signoff and decrease in late-stage design iterations have been found to outweigh the costs. Moreover, the findings of this project are consistent with the literature findings on the advanced technology node, which supports the feasibility and scalability of SI-based routing strategies to obtain stable timing closure in high-performance integrated circuits.

8.3 Guidelines for Routing Strategy Selection

According to the final implementation of the SI block at the 28 nm technology node, this work provides the definite recommendations on choosing the right routing strategy. The findings indicate that with designs of moderate routing density and lower operating frequency, traditional timing-based routing can be used to provide timing closure at low computational cost. Conversely, with higher operating frequency and routing congestion, delay variations due to crosstalk were found to have a high influence on timing behavior and signal-integrity-driven routing is necessary. The SI-aware method was found to be especially effective with nets of long parallel run lengths, of high coupling capacitance on timing-critical paths and with tenacious post-route timing violations. By making SI aware in the routing flow, crosstalk-sensitive paths could be identified and mitigated before the routing flow could get stuck on those paths, and the routing flow could be less reliant on engineering change orders being received late. On the whole, the results show that a hybrid routing plan - which incorporates traditional routing in non-critical areas, and SI-based routing in crosstalk-sensitive paths - provides a good compromise between runtime and timing resilience in advanced node technology.

9. Conclusion

This paper was a comparative analysis of the traditional timing-based routing and signal-integrity-based (crosstalk-driven) routing with a realistic crosstalk implementation of 28 nm ASIC. The paper shows that timing routing is a suitable method in reducing nominal delay and wirelength, but it cannot effectively represent the delay variation in data-dependent behavior and noise caused by interconnect coupling in densely routed and high-frequency networks. Crosstalk-driven routing, in contrast, providing explicit interactions between aggressors and victims, coupling capacitance, and switching alignment have great negative impact on timing robustness, and minimizes setup and hold violations at signoff. Despite the fact that the signal-integrity-aware method adds moderate overhead in routing resource and runtime, these expenses are compensated by enhanced predictability, minimal changes in engineering later in the life cycle and accelerated timing convergence. The results confirm that it is necessary to provide the awareness of crosstalk during routing and static timing analysis for realizing reliable timing closure and improved signal integrity for deep sub-micron ASIC designs, especially at advanced technology nodes like 28 nm.

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